CHAIR FOR COMPILER CONSTRUCTION

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Portable Libraries and Programming Environments

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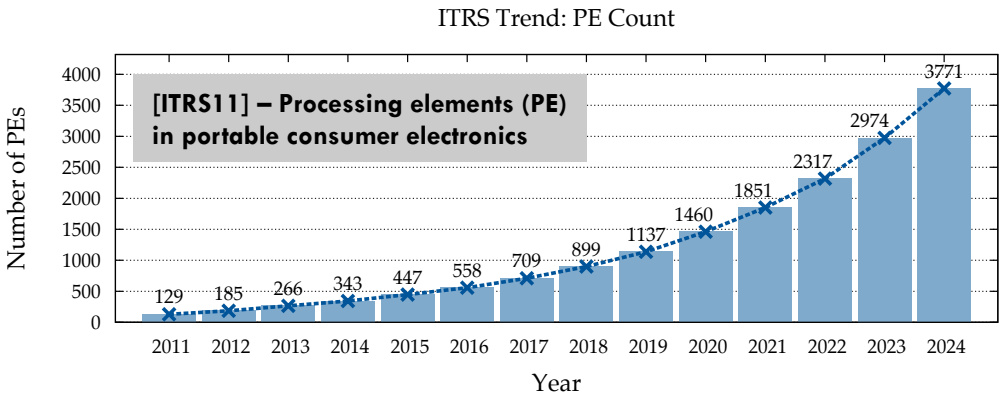
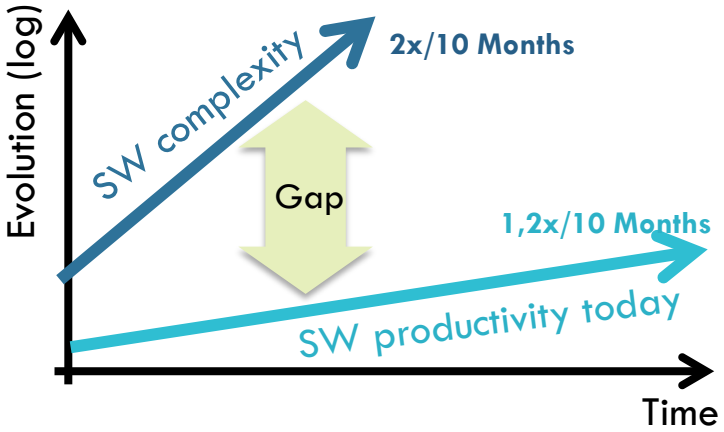
Why new programming environments?



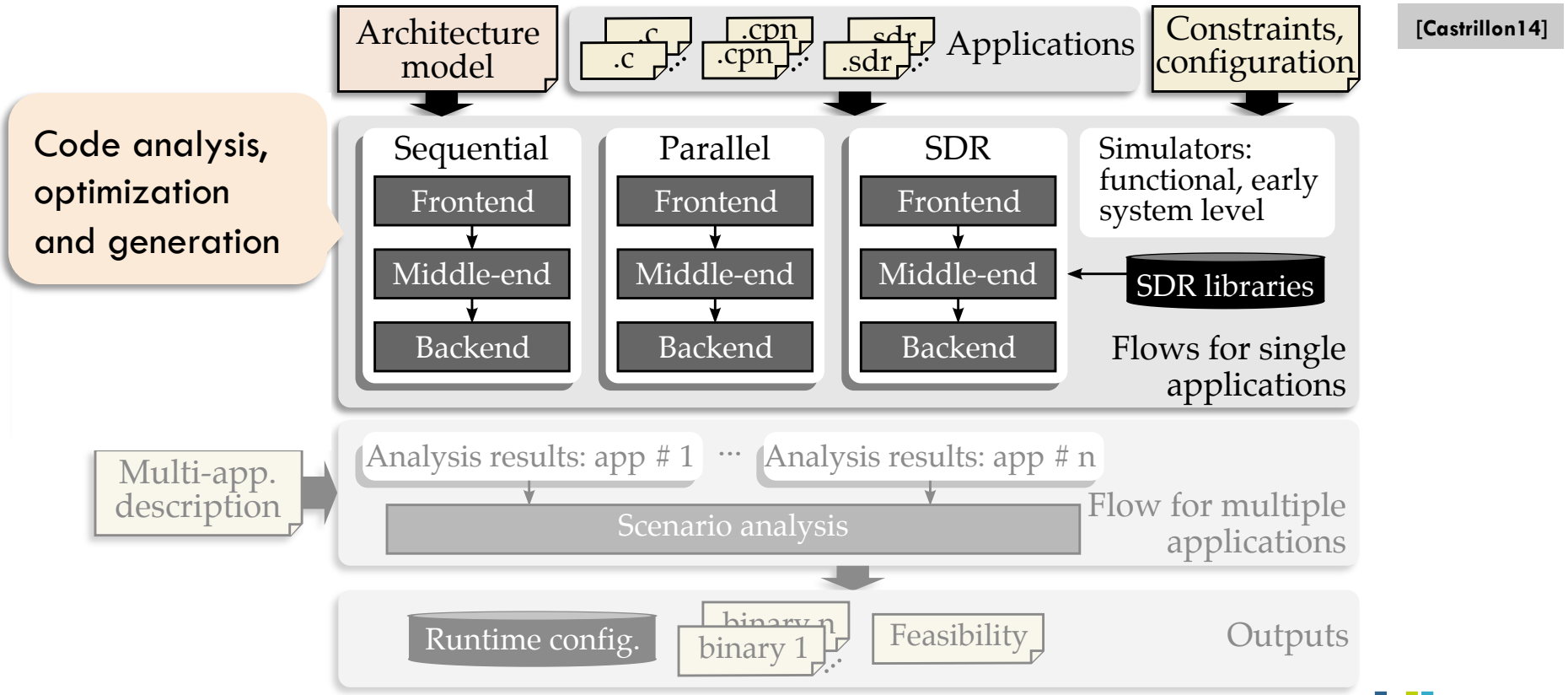


- Complex applications for complex architectures ➔ SW-productivity gap

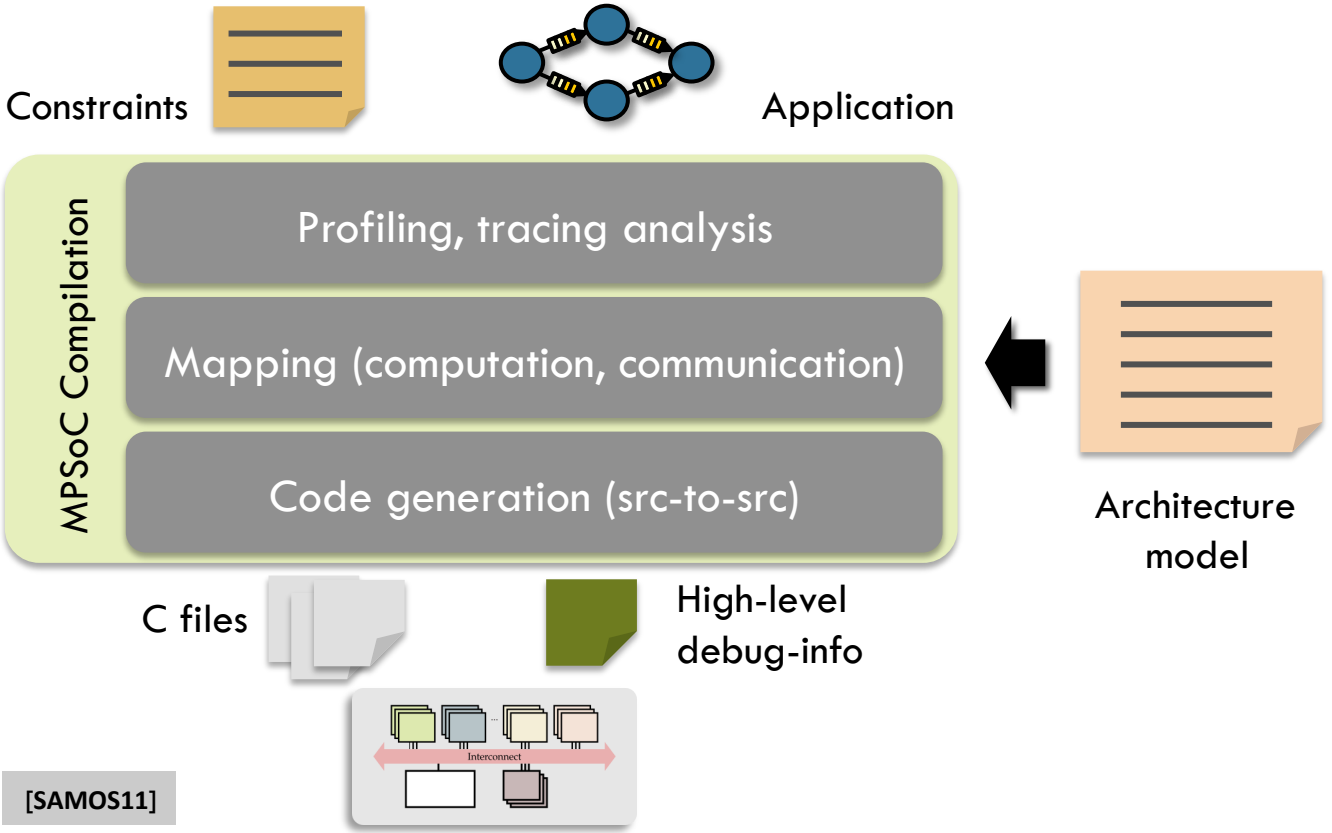
- Already difficult for heterogeneous multi-core (programmable) systems
- More difficult for systems with hardware accelerators and reconfigurable HW

Programming flows for heterogeneous MPSoCs

[Castrillon14]

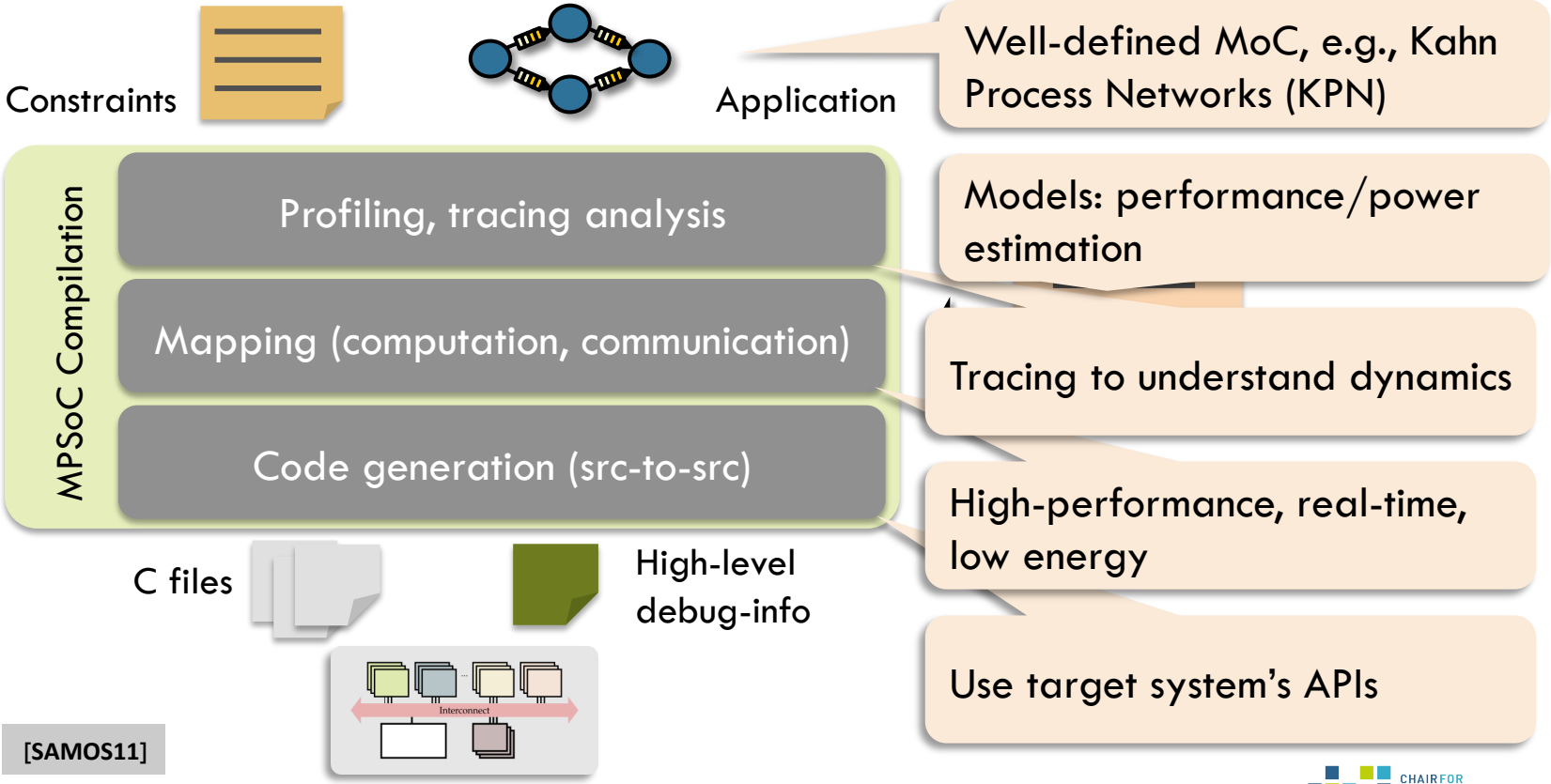


Parallel programming flow: Overview



[SAMOS11]

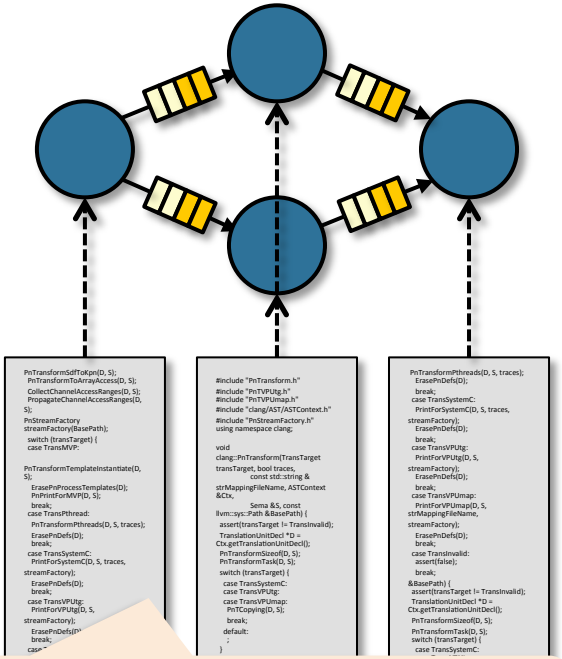
Parallel programming flow: Overview



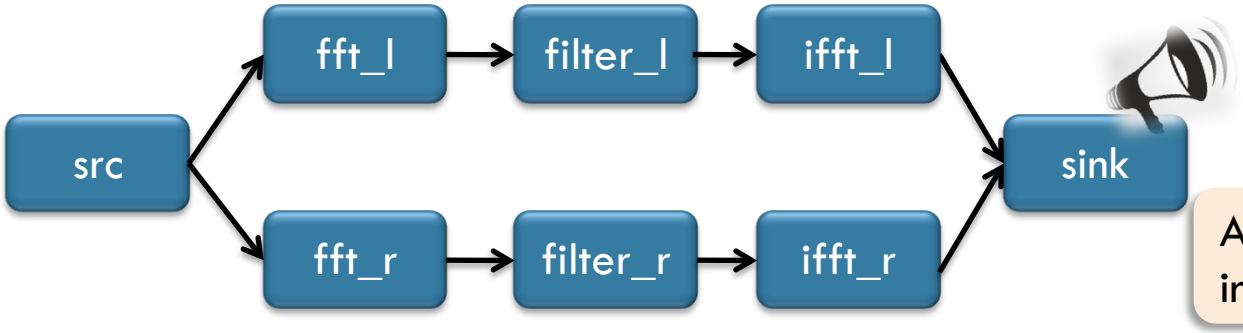
[SAMOS11]

Application: Dataflow and process networks

- Graph representation of applications
  - Process **communicate only** over FIFO buffers
  - Good model for streaming applications
  - Good match for signal processing & multi-media



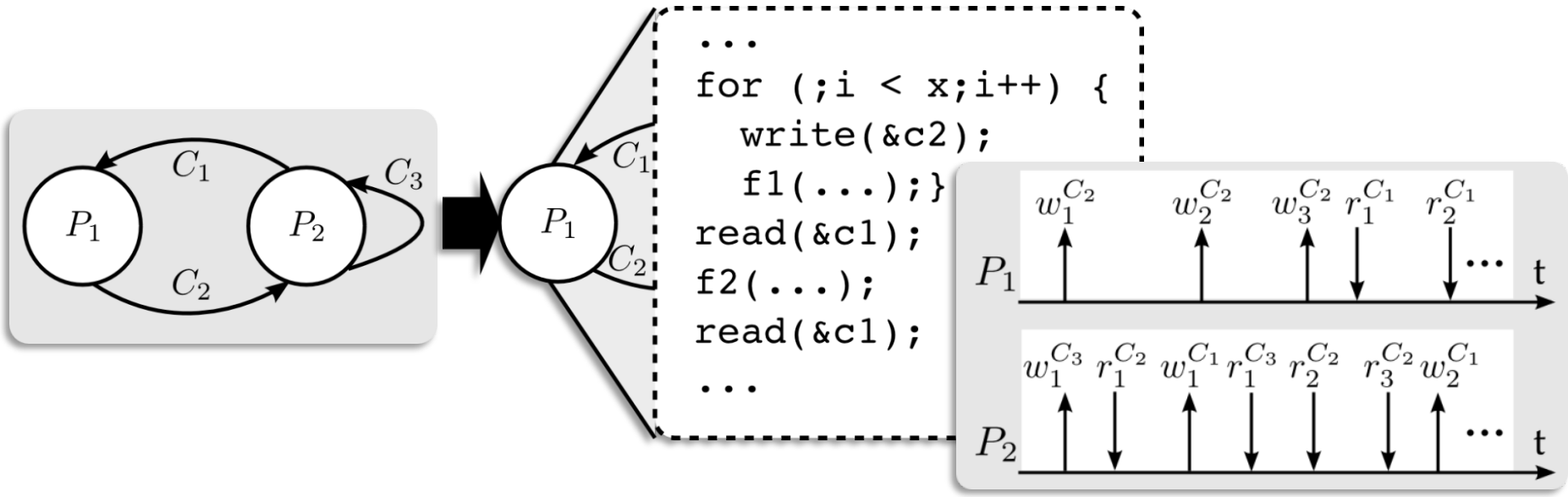
- Stereo digital audio filter



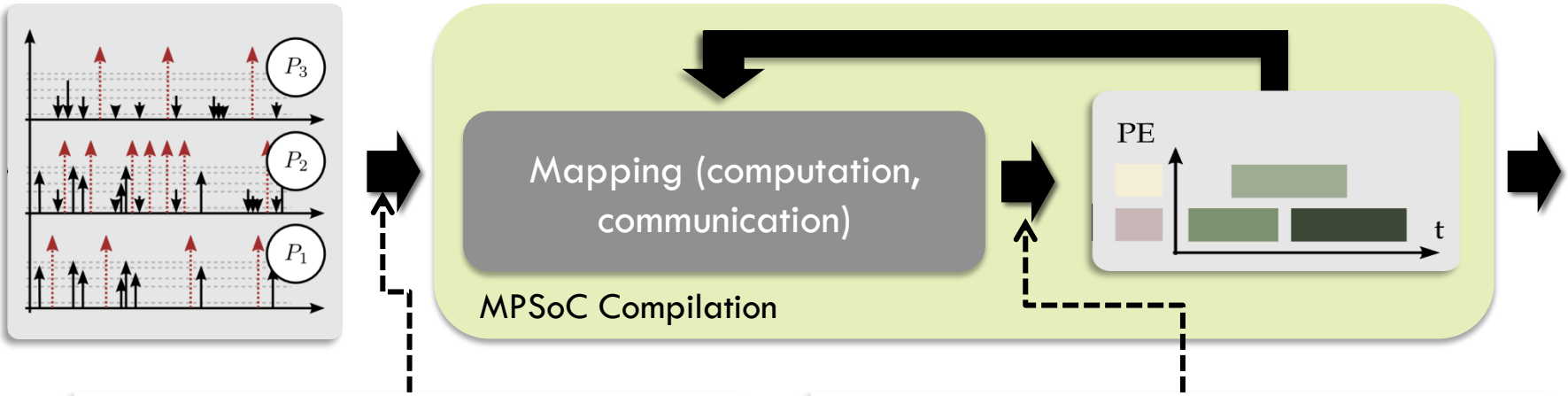
Allows control decision upon incoming data

Analysis: Instrumentation, profiling and tracing

- **Process white model**: source code analysis and tracing to deal with control



Performance models: Sequential and parallel



Sequential performance estimation

Design

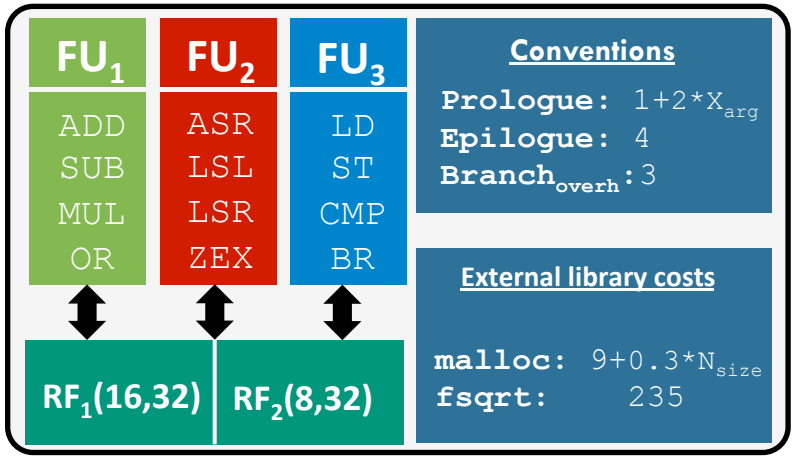
- Annotations & cost functions
- Abstract operation cost models
- Processor models/simulators
- Measurements

Parallel performance estimation

- Abstract cost models: OS, multi-tasking APIs, interconnect & memories
- System simulators/emulators
- Boards

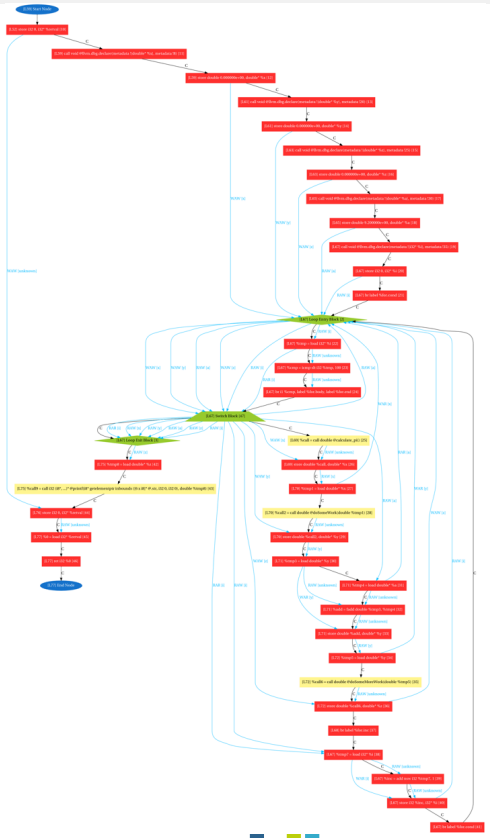
Performance estimation: Computation

- Cost tables
  - Equivalence: Low-level IR → Assembly instructions
  - Coarse estimation of instruction-level parallelism
- Processor + compiler models
  - Set of resources, operations, low-level APIs



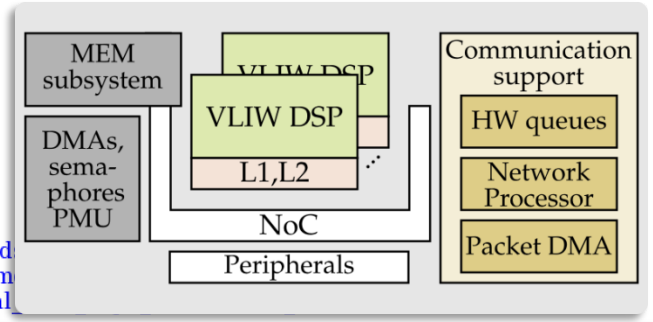
[SAMOS14]

Courtesy: J. Esse

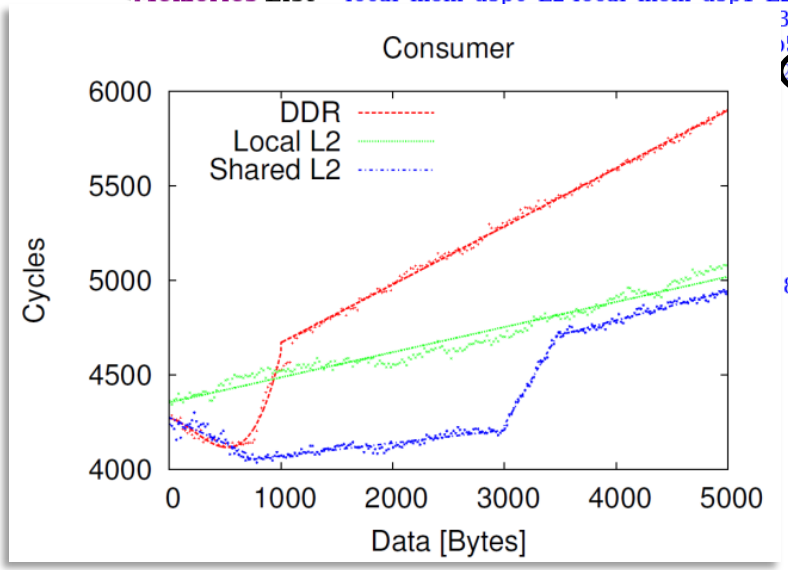


Performance estimation: Communication

- Characterization of different communication APIs
- Example: TI Keystone II



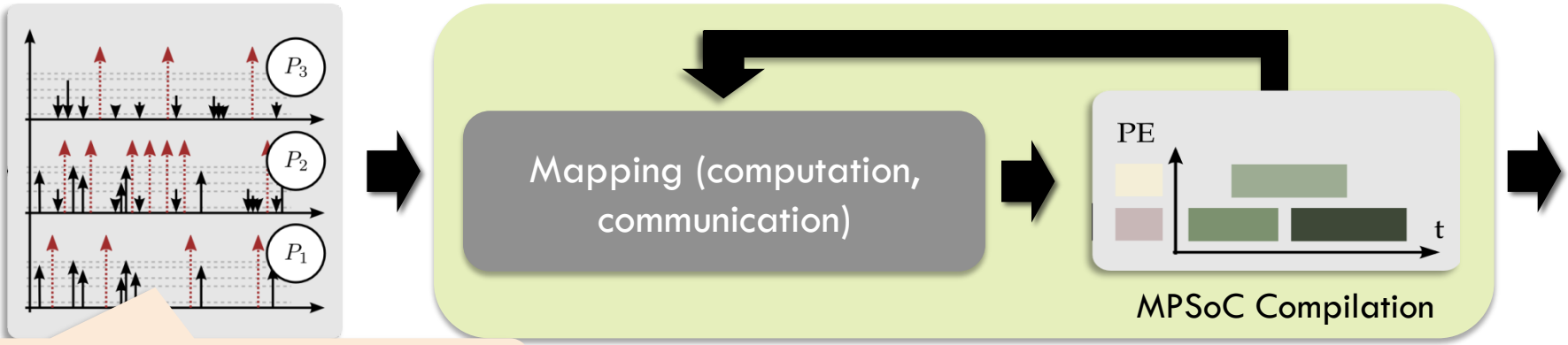

```
−<Platform>
  <Processors List="dsp0 dsp1 dsp2 dsp3 dsp4 dsp5 dsp6 dsp7"/>
  <Memories List="local_mem_dsp0_L2 local_mem_dsp1_L2 local_mem_dsp2_L2 local_mem_d
```




```
−<CommPrimitive>
 −<CPDMA Name="EDMA3_DDR">
    <Description>EDMA over DDR</Description>
   −<Costs>
      <Cost End="800" Function="11442.60163-0.15775*x"/>
      <Cost Start="801" Function="11204.94186+0.316143*x"/>
    </Costs>
    <DMAs List="local_mem_dsp0_DDR local_mem_dsp1_DDR local_
  </CPDMA>
</CommPrimitive>
```

[SOC13]

Application mapping: Trace-based

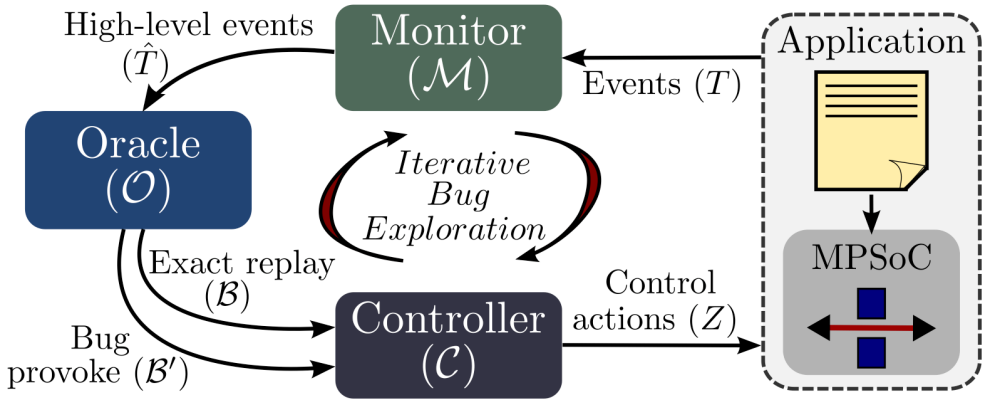


- Heuristics that work on a graph-representation of multiple-traces
  - For buffer sizing
  - For mapping and scheduling
  - Often iterative for real-time

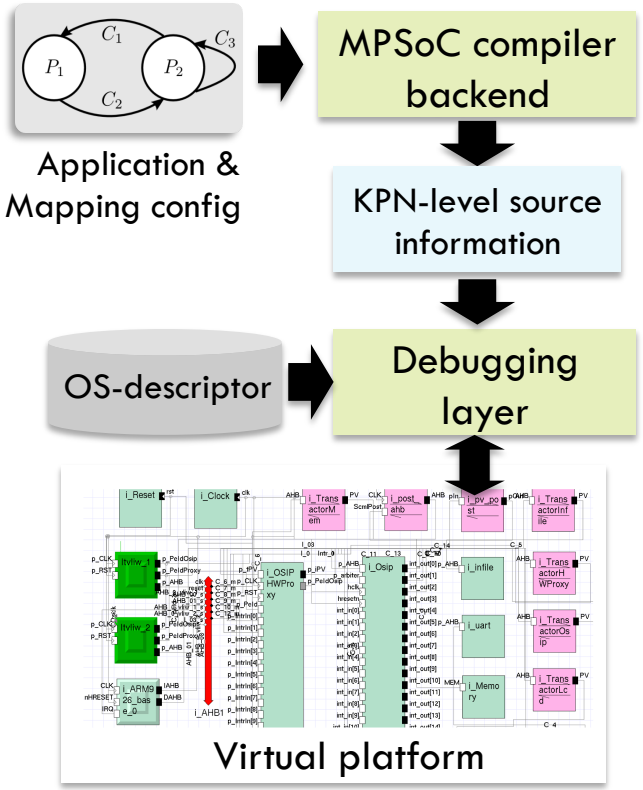
[DATE10, DAC12, IEEE-TII13]

Debugging: Layers and scripting for virtual platforms

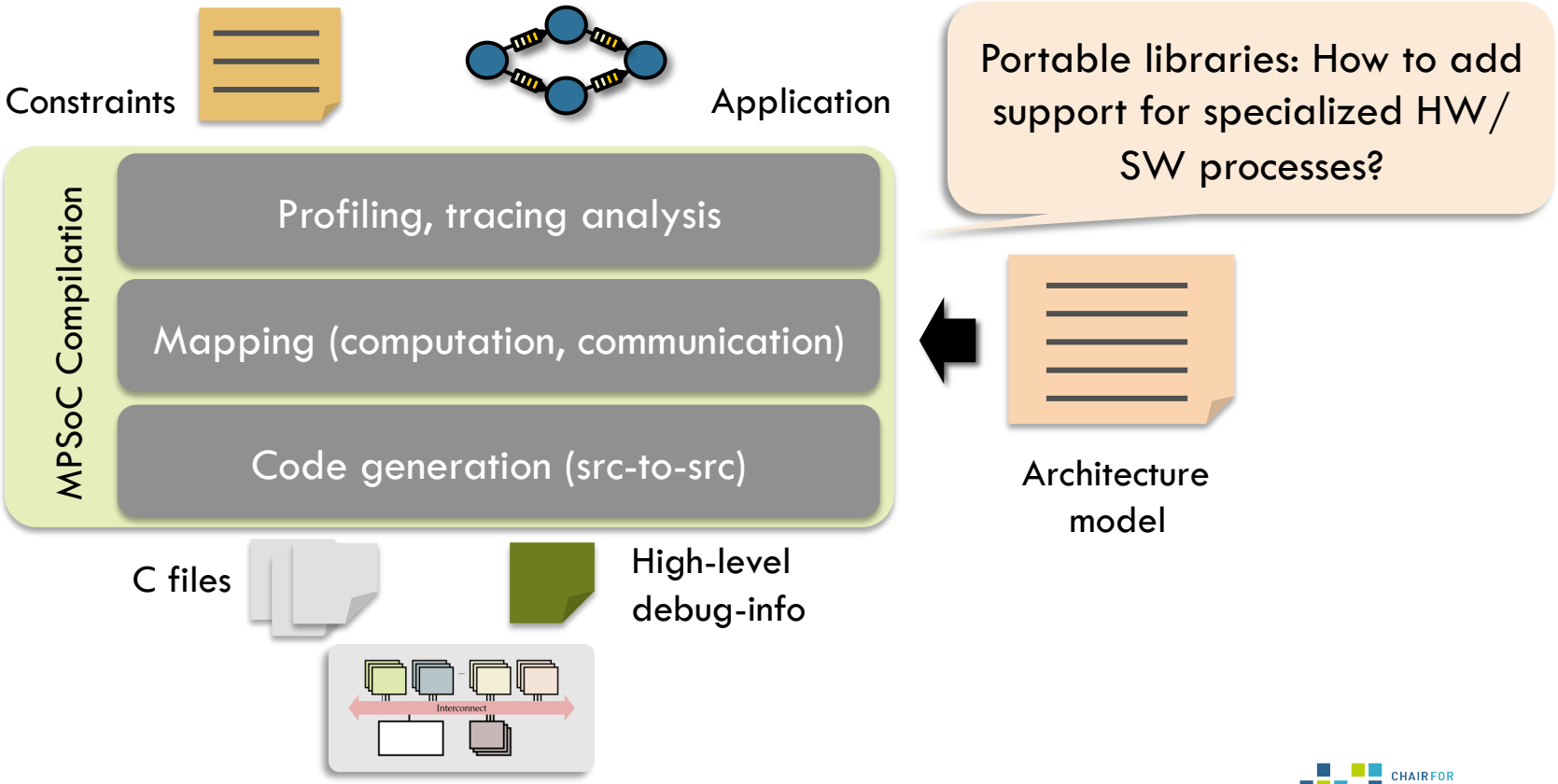
- Interactive debugging
- Deterministic replay for bug exploration



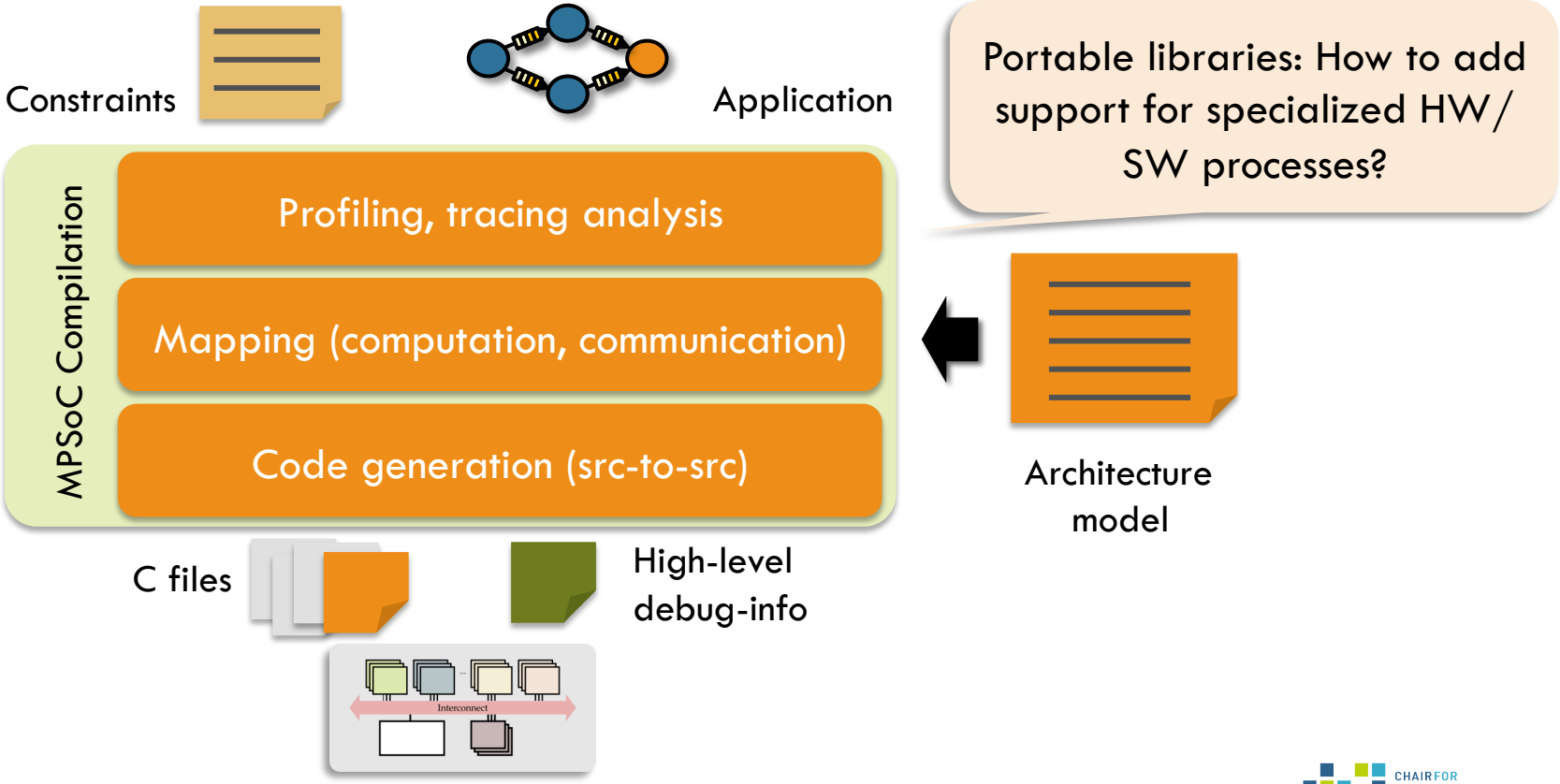
[LASCAS10, DATE14]



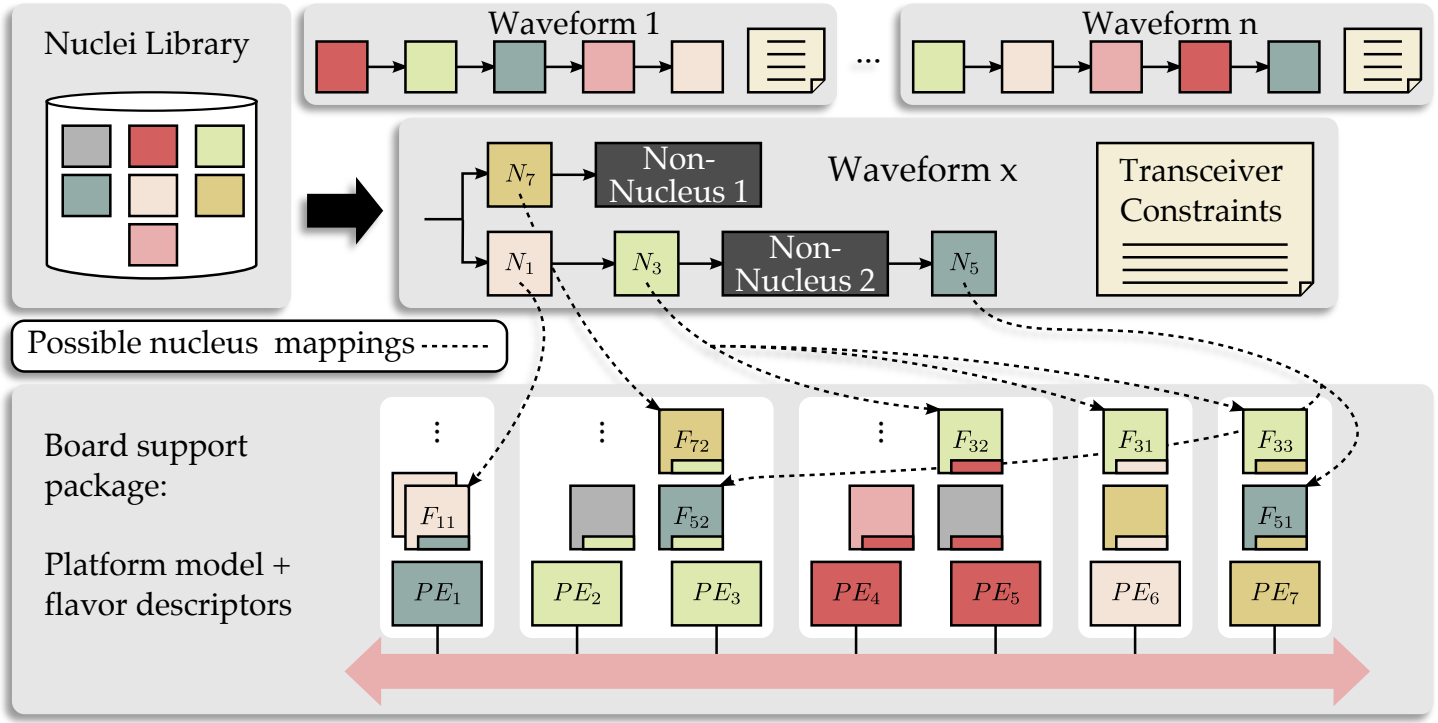
Parallel programming flow: Portable libraries



Parallel programming flow: Portable libraries

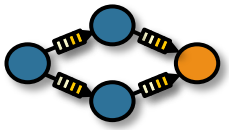


Solution approach: Nucleus project (for SW-defined Radio)



[SDR10, ALOG11,Castrillon14]

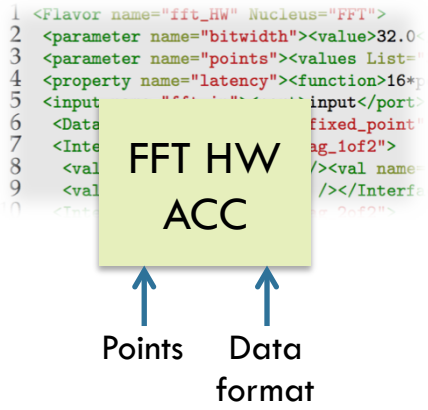
Nucleus programming flow: Inputs



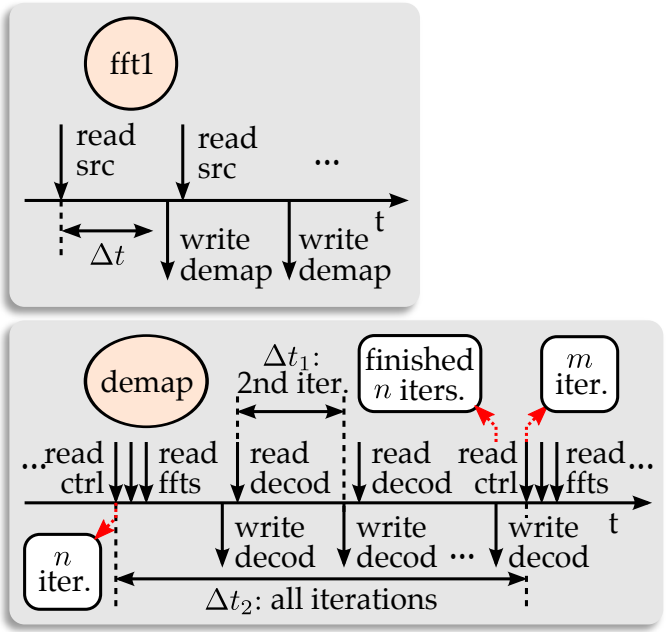
- Extended application specification
  - Selected processes are algorithmic kernels with **algorithmic parameters**
- Extended platform model
  - SW/HW accelerated kernels and their **implementation parameters**

Nucleus programming flow: Mapping

- Extended mapping
  - Find matching HW/SW support: Algorithmic to implementation parameters
  - Integrate into trace-based framework

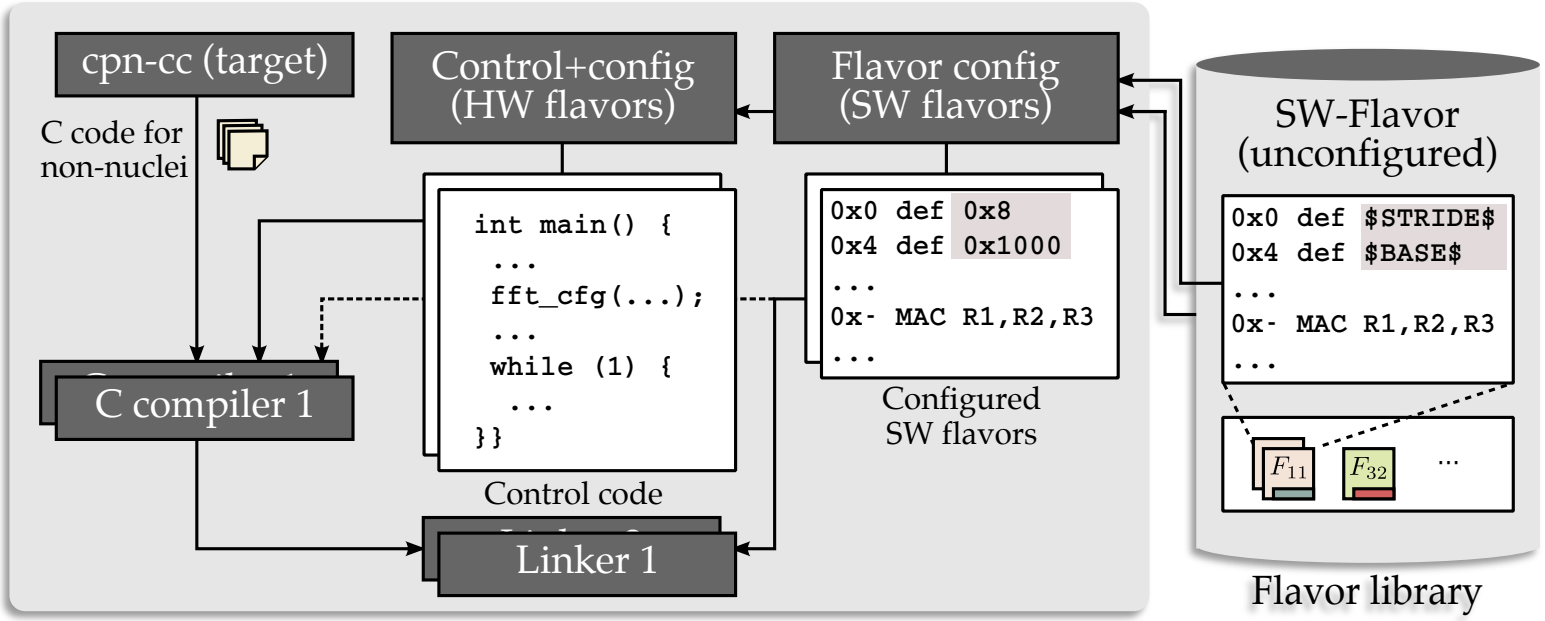


Configuration, characterization



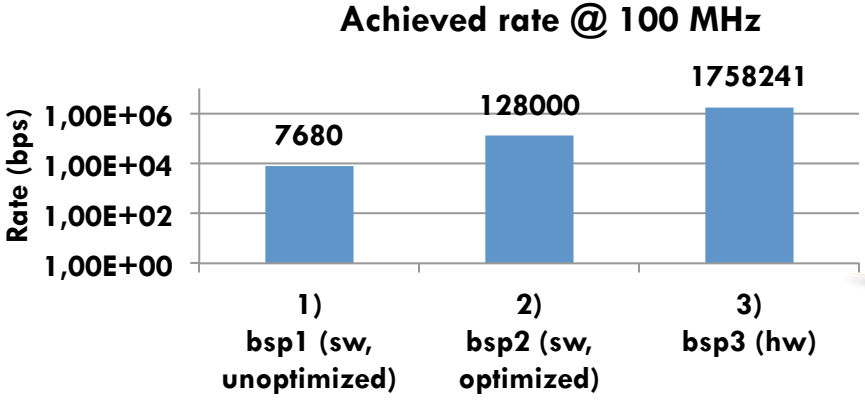
Nucleus programming flow: Code generation

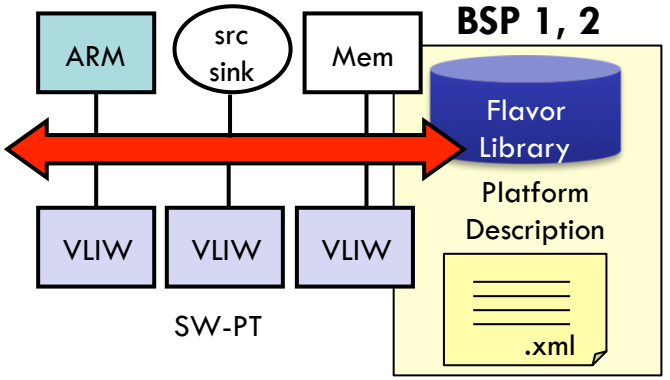
- Bare-metal implementation

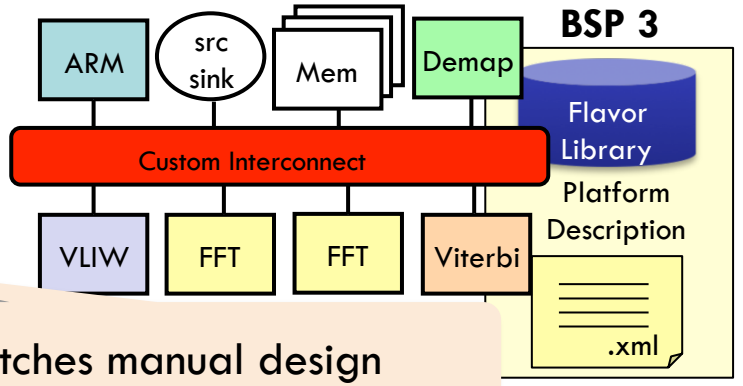


Case study (brief): Portable performance

- Application: MIMO OFDM receiver
- Hardware
  - Platform 1: Baseline software
  - Platform 2: Optimized software
  - Platform 3: Optimized SW + HW







Matches manual design

Discussion towards library portability

- Programming flow extension to deal with HW/SW acceleration
- Desired library characterization (standards?)
  - For mapping
    - Times, data-types, rates (and more complex behaviors – time diagrams?)
  - For debugging
    - Debugging interfaces and true integration (so far: bare metal)
    - Interfacing patterns to be proven by trace analysis
  - For code generation (so far: bare metal)
    - OS integration, interaction with resource manager
- Not addressed: Reconfiguration & synthesis

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