

Dataflow Models of Computation for Programming Heterogeneous Multicores

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Abstract The hardware complexity of modern integrated circuits keeps increasing at a steady pace. Heterogeneous Multi-Processor Systems-on-Chips (MPSoCs) integrate general purpose processing elements, domain-specific processors, dedicated hardware accelerators, reconfigurable logic, as well as complex memory hierarchies and interconnect. While offering unprecedented computational power and energy efficiency, MPSoCs are notoriously difficult to program. This chapter presents Models of Computation (MoCs) as an appealing alternative to traditional programming methodologies to harness the full capacities of modern MPSoCs. By raising the level of abstraction, MoCs make it possible to specify complex systems with little knowledge of the target architecture. The properties of MoCs make it possible for tools to automatically generate efficient implementations for heterogeneous MPSoCs, relieving developers from time consuming manual exploration. This chapter focuses on a specific MoC family called dataflow MoCs. Dataflow MoCs represent systems as graphs of computational entities and communication channels. This graph-based system specification enables intuitive description of parallelism, and supports many analysis and optimization techniques for deriving safe and highly efficient implementations on MPSoCs.

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References

- [1] Reinhard Wilhelm, Jakob Engblom, Andreas Ermedahl, Niklas Holsti, Stephan Thesing, et al. “The Worst-case Execution-time Problem—Overview of Methods and Survey of Tools”. In: *ACM Trans. Embed. Comput. Syst.* 7.3 (2008), pp. 1–53. issn: 1539-9087. doi: <http://doi.acm.org/10.1145/1347375.1347389>.
- [2] Xavier Leroy. “Formal verification of a realistic compiler”. In: *Communications of the ACM* 52.7 (2009), pp. 107–115.
- [3] Rajeev Alur, Costas Courcoubetis, and David Dill. “Model-checking for real-time systems”. In: *[1990] Proceedings. Fifth Annual IEEE Symposium on Logic in Computer Science*. IEEE, 1990, pp. 414–425.
- [4] Phil Rogers and A Fellow. “Heterogeneous system architecture overview.” In: *Hot Chips Symposium*. 2013, pp. 1–41.
- [5] Urs Gleim and Markus Levy. “MTAPI: parallel programming for embedded multicore systems”. In: *The Multicore Association* (2013).
- [6] Edward A Lee. “The problem with threads”. In: *Computer* 39.5 (2006), pp. 33–42.
- [7] Jianjiang Ceng, Jeronimo Castrillon, Weihua Sheng, Hanno Scharwächter, Rainer Leupers, et al. “MAPS: An Integrated Framework for MPSoC Application Parallelization”. In: *Proceedings of the 45th Annual Design Automation Conference*. DAC’08. Anaheim, California: ACM, June 2008, pp. 754–759. isbn: 978-1-60558-115-6. doi: [10.1145/1391469.1391663](http://doi.acm.org/10.1145/1391469.1391663). url: <http://doi.acm.org/10.1145/1391469.1391663>.
- [8] Maxime Pelcat, Karol Desnos, Julien Heulot, Clément Guy, Jean-François Nezan, and Slaheddine Aridhi. “Preesm: A dataflow-based rapid prototyping framework for simplifying multicore dsp programming”. In: *2014 6th european embedded design in education and research conference (EDERC)*. IEEE, 2014, pp. 36–40.
- [9] Axel Jantsch. *Modeling Embedded Systems and SoC’s: Concurrency and Time in Models of Computation*. Elsevier, 2003.
- [10] Alonzo Church. *The calculi of lambda-conversion*. No. 6. Princeton University Press, 1985.
- [11] Edward Ashford Lee and Sanjit A Seshia. *Introduction to embedded systems: A cyber-physical systems approach*. Mit Press, 2016.
- [12] John L Kelly, Carol Lochbaum, and Victor A Vyssotsky. “A block diagram compiler”. In: *The Bell System Technical Journal* 40.3 (1961), pp. 669–678.
- [13] Gilles Kahn. “The semantics of a simple language for parallel programming”. In: *Information processing 74* (1974), pp. 471–475.
- [14] Jack B. Dennis. “First version of a data flow procedure language”. In: *Programming Symposium*. Ed. by B. Robinet. Berlin, Heidelberg: Springer Berlin Heidelberg, 1974, pp. 362–376. isbn: 978-3-540-37819-8.
- [15] Edward A Lee and David G Messerschmitt. “Synchronous data flow”. In: *Proceedings of the IEEE* 75.9 (1987), pp. 1235–1245.
- [16] Wolfgang Ecker, Wolfgang Müller, and Rainer Dömer. “Hardware-dependent software”. In: *Hardware-dependent Software*. Springer, 2009, pp. 1–13.
- [17] Edward A Lee and Soonhoi Ha. “Scheduling strategies for multiprocessor real-time DSP”. In: *1989 IEEE Global Telecommunications Conference and Exhibition: Communications Technology for the 1990s and Beyond’*. IEEE, 1989, pp. 1279–1283.

- [18] Karol Desnos, Maxime Pelcat, Jean-François Nezan, and Slaheddine Aridhi. “Memory analysis and optimized allocation of dataflow applications on shared-memory mpsocs”. In: *Journal of Signal Processing Systems* 80.1 (2015), pp. 19–37.
- [19] Edward Ashford Lee and David G Messerschmitt. “Static scheduling of synchronous data flow programs for digital signal processing”. In: *IEEE Transactions on computers* 100.1 (1987), pp. 24–35.
- [20] Jose Luis Pino, Shuvra S Bhattacharyya, and Edward A Lee. “A hierarchical multiprocessor scheduling system for DSP applications”. In: *Conference Record of The Twenty-Ninth Asilomar Conference on Signals, Systems and Computers*. Vol. 1. IEEE. 1996, pp. 122–126.
- [21] Greet Bilsen, Marc Engels, Rudy Lauwereins, and Jean Peperstraete. “Cycle-static dataflow”. In: *IEEE Transactions on signal processing* 44.2 (1996), pp. 397–408.
- [22] Adnan Bouakaz, Jean-Pierre Talpin, and Jan Vitek. “Affine data-flow graphs for the synthesis of hard real-time applications”. In: *2012 12th International Conference on Application of Concurrency to System Design*. IEEE. 2012, pp. 183–192.
- [23] J. Piat, S. S. Bhattacharyya, and M. Raullet. “Interface-based hierarchy for synchronous data-flow graphs”. In: *2009 IEEE Workshop on Signal Processing Systems*. 2009, pp. 145–150. doi: [10.1109/SIPS.2009.5336240](https://doi.org/10.1109/SIPS.2009.5336240).
- [24] Joachim Keinert, Christian Haubelt, and Jürgen Teich. “Windowed synchronous data flow”. In: *Department of Computer Science* 12 (2005).
- [25] Joseph T. Buck. “Scheduling Dynamic Dataflow Graphs with Bounded Memory Using the Token Flow Model”. PhD thesis. EECS Department, University of California, Berkeley, Sept. 1993. URL: <http://www2.eecs.berkeley.edu/Pubs/TechRpts/1993/2429.html>.
- [26] Gilles Kahn and David MacQueen. “Coroutines and networks of parallel processes”. In: (1976).
- [27] Edward A Lee and Thomas M Parks. “Dataflow process networks”. In: *Proceedings of the IEEE* 83.5 (1995), pp. 773–801.
- [28] Johan Eker and Jorn Janneck. *CAL language report*. Tech. rep. Tech. Rep. ERL Technical Memo UCB/ERL, 2003.
- [29] H. Yviquel, A. Lorence, K. Jerbi, G. Cocherel, A. Sanchez, and M. Raullet. “Orcc: Multimedia Development Made Easy”. In: *Proceedings of the 21st ACM International Conference on Multimedia*. MM ’13. Barcelona, Spain: ACM, 2013, pp. 863–866. ISBN: 978-1-4503-2404-5. doi: [10.1145/2502081.2502231](https://doi.org/10.1145/2502081.2502231). URL: <http://doi.acm.org/10.1145/2502081.2502231>.
- [30] Shuvra S Bhattacharyya, Gordon Brebner, Jörn W Janneck, Johan Eker, Carl Von Platen, Marco Mattavelli, and Mickaël Raullet. “OpenDF: a dataflow toolset for reconfigurable hardware and multicore systems”. In: *ACM SIGARCH Computer Architecture News* 36.5 (2009), pp. 29–35.
- [31] Sander Stuijk, Marc Geilen, Bart Theelen, and Twan Basten. “Scenario-aware dataflow: Modeling, analysis and implementation of dynamic applications”. In: *2011 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation*. IEEE. 2011, pp. 404–411.
- [32] S. Neuendorffer and E.A. Lee. “Hierarchical reconfiguration of dataflow models”. In: *MEMOCODE*. 2004. doi: [10.1109/MEMCOD.2004.1459852](https://doi.org/10.1109/MEMCOD.2004.1459852).
- [33] Karol Desnos, Maxime Pelcat, Jean-François Nezan, Shuvra S Bhattacharyya, and Slaheddine Aridhi. “Pimm: Parameterized and interfaced dataflow meta-model for mpsocs runtime reconfiguration”. In: *2013 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)*. IEEE. 2013, pp. 41–48.
- [34] Bishnupriya Bhattacharya and Shuvra S Bhattacharyya. “Parameterized dataflow modeling for DSP systems”. In: *IEEE Transactions on Signal Processing* 49.10 (2001), pp. 2408–2421.
- [35] Pascal Fradet, Alain Girault, Ruby Krishnaswamy, Xavier Nicollin, and Arash Shafiei. *RDF: Reconfigurable Dataflow (extended version)*. Tech. rep. INRIA Grenoble-Rhône-Alpes, 2018.
- [36] Vagelis Bebelis, Pascal Fradet, Alain Girault, and Bruno Lavigueur. “BPDF: A statically analyzable dataflow model with integer and boolean parameters”. In: *2013 Proceedings of the International Conference on Embedded Software (EMSOFT)*. IEEE. 2013, pp. 1–10.
- [37] Mickaël Dardaillon, Kevin Marquet, Tanguy Risset, Jérôme Martin, and Henri-Pierre Charles. “A new compilation flow for software-defined radio applications on heterogeneous MPSoCs”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 13.2 (2016), pp. 1–25.
- [38] Shuoxin Lin, Lai-Huei Wang, Aida Vosoughi, Joseph R Cavallaro, Markku Juntti, et al. “Parameterized sets of dataflow modes and their application to implementation of cognitive radio systems”. In: *Journal of Signal Processing Systems* 80.1 (2015), pp. 3–18.

- [39] Peter Marwedel, Iuliana Bacivarov, Chanhee Lee, Jürgen Teich, Lothar Thiele, et al. “Mapping of Applications to MPSoCs”. In: *Proceedings of the 9th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*. Oct. 2011, pp. 109–118.
- [40] Eric Biscondi, Tom Flanagan, Frank Fruth, Zhihong Lin, and Filip Moerman. *Maximizing Multicore Efficiency with Navigator Runtime*. White Paper. Feb. 2012. URL: www.ti.com/lit/wp/spr190/spr190.pdf.
- [41] Andrea Pellegrini, Nigel Stephens, Magnus Bruce, Yasuo Ishii, Joseph Pusdesris, et al. “The Arm Neoverse N1 Platform: Building Blocks for the Next-Gen Cloud-to-Edge Infrastructure SoC”. In: *IEEE Micro* 40.2 (2020), pp. 53–62.
- [42] Benoit Dupont de Dinechin. “Kalray MPPA®: Massively parallel processor array: Revisiting DSP acceleration with the Kalray MPPA manycore processor”. In: *2015 IEEE Hot Chips 27 Symposium (HCS)*. IEEE. 2015, pp. 1–27.
- [43] A.D. Pimentel, C. Erbas, and S. Polstra. “A systematic approach to exploring embedded system architectures at multiple abstraction levels”. In: *IEEE Transactions on Computers* 55.2 (Feb. 2006), pp. 99–112. ISSN: 0018-9340. DOI: [10.1109/TC.2006.16](https://doi.org/10.1109/TC.2006.16).
- [44] Lothar Thiele, Iuliana Bacivarov, Wolfgang Haid, and Kai Huang. “Mapping Applications to Tiled Multiprocessor Embedded Systems”. In: *ACSD '07: Proceedings of the Seventh International Conference on Application of Concurrency to System Design*. Washington, DC, USA: IEEE Computer Society, 2007, pp. 29–40. ISBN: 0-7695-2902-X. DOI: <http://dx.doi.org/10.1109/ACSD.2007.53>.
- [45] Maxime Pelcat, Pierrick Menuet, Slaheddine Aridhi, and Jean-François Nezan. “Scalable compile-time scheduler for multi-core architectures”. In: *2009 Design, Automation & Test in Europe Conference & Exhibition*. IEEE. 2009, pp. 1552–1555.
- [46] Simone Casale Brunet, Claudio Alberti, Marco Mattavelli, and Jörn Janneck. “Turnus: a unified dataflow design space exploration framework for heterogeneous parallel systems”. In: *2013 conference on design and architectures for signal and image processing (DASIP)*. 2013, pp. 47–54.
- [47] Juan Fernando Eusse, Christopher Williams, and Rainer Leupers. “CoEx: A Novel Profiling-Based Algorithm/Architecture Co-Exploration for ASIP Design”. In: *ACM Transactions on Reconfigurable Technology and Systems* (May 2014). DOI: [10.1109/ReCoSoC.2013.6581520](https://doi.org/10.1109/ReCoSoC.2013.6581520).
- [48] C/DA - Design Automation. “IEEE Standard for Software-Hardware Interface for Multi-Many-Core”. In: *IEEE Std 2804-2019* (Jan. 2020), pp. 1–84. DOI: [10.1109/IEEESTD.2020.8985663](https://doi.org/10.1109/IEEESTD.2020.8985663). URL: <https://standards.ieee.org/standard/2804-2019.html>.
- [49] Jeronimo Castrillon, Andreas Tretter, Rainer Leupers, and Gerd Ascheid. “Communication-aware Mapping of KPN Applications Onto Heterogeneous MPSoCs”. In: *Proceedings of the 49th Annual Design Automation Conference*. DAC '12. San Francisco, California: ACM, June 2012, pp. 1266–1271. ISBN: 978-1-4503-1199-1. DOI: [10.1145/2228360.2228597](https://doi.org/10.1145/2228360.2228597). URL: <http://doi.acm.org/10.1145/2228360.2228597>.
- [50] The Multicore Association, Inc. *Software-Hardware Interface for Multi-Many-Core (SHIM) Specification, V1.0*. The Multicore Association, Inc. Jan. 2015.
- [51] Rainer Leupers, Miguel Angel Aguilar, Juan Fernando Eusse, Jeronimo Castrillon, and Weihua Sheng. “MAPS: A Software Development Environment for Embedded Multicore Applications”. In: *Handbook of Hardware/Software Codesign*. Ed. by Soonhoi Ha and Jürgen Teich. Dordrecht: Springer Netherlands, Apr. 2017, pp. 1–33. ISBN: 978-94-017-7358-4. DOI: [10.1007/978-94-017-7358-4_2-1](https://doi.org/10.1007/978-94-017-7358-4_2-1). URL: http://dx.doi.org/10.1007/978-94-017-7358-4_2-1.
- [52] Christian Menard, Andrés Goens, Gerald Hempel, Robert Khasanov, Julian Robledo, Felix Teweleit, and Jeronimo Castrillon. “Mocasin—Rapid Prototyping of Rapid Prototyping Tools: A Framework for Exploring New Approaches in Mapping Software to Heterogeneous Multi-cores”. In: *DroneSE and RAPIDO 2021, System Engineering for constrained embedded systems*. RAPIDO '21. Virtual event, Jan. 2021. DOI: [10.1145/3444950.344728](https://doi.org/10.1145/3444950.344728).
- [53] M. Pelcat, K. Desnos, L. Maggiani, Y. Liu, J. Heulot, J. Nezan, and S. S. Bhattacharyya. “Models of Architecture: Reproducible Efficiency Evaluation for Signal Processing Systems”. In: *2016 IEEE International Workshop on Signal Processing Systems (SiPS)*. Oct. 2016, pp. 121–126. DOI: [10.1109/SiPS.2016.29](https://doi.org/10.1109/SiPS.2016.29).
- [54] M. Pelcat, A. Mercat, K. Desnos, L. Maggiani, Y. Liu, et al. “Reproducible Evaluation of System Efficiency With a Model of Architecture: From Theory to Practice”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 37.10 (2018), pp. 2050–2063. DOI: [10.1109/TCAD.2017.2774822](https://doi.org/10.1109/TCAD.2017.2774822).
- [55] Andreas Gerstlauer, Christian Haubelt, Andy D Pimentel, Todor P Stefanov, Daniel D Gajski, and Jürgen Teich. “Electronic system-level synthesis methodologies”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 28.10 (2009), pp. 1517–1530.

- [56] Kai Huang, Wolfgang Haid, Iuliana Bacivarov, Matthias Keller, and Lothar Thiele. “Embedding Formal Performance Analysis into the Design Cycle of MPSoCs for Real-time Streaming Applications”. In: *ACM Transactions in Embedded Computing Systems (TECS)* (2012).
- [57] Lothar Thiele, Samarjit Chakraborty, and Martin Naedele. “Real-time calculus for scheduling hard real-time systems”. In: *2000 IEEE International Symposium on Circuits and Systems (ISCAS)*. Vol. 4. IEEE. 2000, pp. 101–104.
- [58] Andreas Tretter. “On Efficient Data Exchange in Multicore Architectures”. PhD thesis. ETH Zurich, Dec. 2018, 206 pp. URL: <https://www.research-collection.ethz.ch/handle/20.500.11850/309314>.
- [59] Y. Lesparre, A. Munier-Kordon, and J. Delosme. “Evaluation of Synchronous Dataflow Graph Mappings onto Distributed Memory Architectures”. In: *2016 Euromicro Conference on Digital System Design (DSD)*. 2016, pp. 146–153. doi: [10.1109/DSD.2016.52](https://doi.org/10.1109/DSD.2016.52).
- [60] Alemeh Ghasemi, Rodrigo Cataldo, Jean-Philippe Diguët, and Kevin JM Martin. “On Cache Limits for Dataflow Applications and Related Efficient Memory Management Strategies”. In: *Workshop on Design and Architectures for Signal and Image Processing (14th edition)*. 2021, pp. 68–76.
- [61] Lei Gao, Jia Huang, Jianjiang Ceng, Rainer Leupers, Gerd Ascheid, and Heinrich Meyr. “TotalProf: a Fast and Accurate Retargetable Source Code Profiler”. In: *CODES+ISSS '09: Proceedings of the 7th IEEE/ACM international conference on Hardware/software codesign and system synthesis*. Grenoble, France: ACM, 2009, pp. 305–314. ISBN: 978-1-60558-628-1. DOI: <http://doi.acm.org/10.1145/1629435.1629477>.
- [62] Ralf Stemmer, Hai-Dang Vu, Kim Grüttner, Sébastien Le Nours, Wolfgang Nebel, and Sébastien Pillement. “Towards Probabilistic Timing Analysis for SDFGs on Tile Based Heterogeneous MPSoCs”. In: 2020.
- [63] Charith Mendis, Alex Renda, Saman Amarasinghe, and Michael Carbin. “Ithemal: Accurate, portable and fast basic block throughput estimation using deep neural networks”. In: *International Conference on Machine Learning*. PMLR, 2019, pp. 4505–4515.
- [64] Peter Van Stralen and Andy D Pimentel. “A high-level microprocessor power modeling technique based on event signatures”. In: *Journal of Signal Processing Systems* 60.2 (2010), pp. 239–250.
- [65] Roberta Piscitelli and Andy D Pimentel. “A high-level power model for mpsoC on fpga”. In: *2011 IEEE International Symposium on Parallel and Distributed Processing Workshops and Phd Forum*. IEEE. 2011, pp. 128–135.
- [66] Stefan Schuermans and Rainer Leupers. *Power estimation on electronic system level using linear power models*. Springer, 2019.
- [67] Kyriakos Georgiou, Steve Kerrison, Zbigniew Chamski, and Kerstin Eder. “Energy transparency for deeply embedded programs”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 14.1 (2017), pp. 1–26.
- [68] Amílcar Meneses-Viveros, Mireya Paredes-López, Erika Hernández-Rubio, and Isidoro Gitler. “Energy consumption model in multicore architectures with variable frequency”. In: *The Journal of Supercomputing* (2020), pp. 1–28.
- [69] Daniel Madronal, Florian Arrestier, Jaime Sancho, Antoine Morvan, Raquel Lazcano, et al. “Papify: Automatic instrumentation and monitoring of dynamic dataflow applications based on papi”. In: *IEEE Access* 7 (2019), pp. 111801–111812.
- [70] Yu-Kwong Kwok and Ishfaq Ahmad. “Static Scheduling Algorithms for Allocating Directed Task Graphs to Multiprocessors”. In: *ACM Comput. Surv.* 31.4 (1999), pp. 406–471. ISSN: 0360-0300. DOI: <http://doi.acm.org/10.1145/344588.344618>.
- [71] Alexandre Honorat, Karol Desnos, Mickaël Dardaillon, and Jean-François Nezan. “A Fast Heuristic to Pipeline SDF Graphs”. In: *Embedded Computer Systems: Architectures, Modeling, and Simulation*. Ed. by Alex Orailoglu, Matthias Jung, and Marc Reichenbach. Cham: Springer International Publishing, 2020, pp. 139–151. ISBN: 978-3-030-60939-9.
- [72] Jeronimo Castrillon, Ricardo Velásquez, Anastasia Stulova, Weihua Sheng, Jianjiang Ceng, et al. “Trace-based KPN Composability Analysis for Mapping Simultaneous Applications to MPSoC Platforms”. In: *Proceedings of the Conference on Design, Automation and Test in Europe*. DATE '10. Dresden, Germany: European Design and Automation Association, Mar. 2010, pp. 753–758. ISBN: 978-3-9810801-6-2. URL: <http://dl.acm.org/citation.cfm?id=1870926.1871107>.
- [73] Peter Van Stralen and Andy D Pimentel. “A trace-based scenario database for high-level simulation of multimedia mp-socs”. In: *2010 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation*. IEEE. 2010, pp. 11–19.
- [74] Jeronimo Castrillon, Rainer Leupers, and Gerd Ascheid. “MAPS: Mapping Concurrent Dataflow Applications to Heterogeneous MPSoCs”. In: *IEEE Transactions on Industrial Informatics* 9.1 (Feb. 2013), pp. 527–545. ISSN: 1551-3203. DOI: [10.1109/TII.2011.2173941](https://doi.org/10.1109/TII.2011.2173941).

- [75] Simone Casale Brunet. “Analysis and optimization of dynamic dataflow programs”. PhD thesis. Ecole Polytechnique Federale de Lausanne (EPFL), 2015.
- [76] Scott Kirkpatrick, C Daniel Gelatt, and Mario P Vecchi. “Optimization by simulated annealing”. In: *science* 220.4598 (1983), pp. 671–680.
- [77] Fred Glover. “Tabu search—part I”. In: *ORSA Journal on computing* 1.3 (1989), pp. 190–206.
- [78] Ilkka Hautala, Jani Boutellier, Teemu Nyländén, and Olli Silvén. “Toward Efficient Execution of RVC-CAL Dataflow Programs on Multicore Platforms”. In: *Journal of Signal Processing Systems* 90 (2018), pp. 1507–1517. ISSN: 1939-8018. DOI: [10.1007/s11265-018-1339-x](https://doi.org/10.1007/s11265-018-1339-x).
- [79] Andreas Weichslgartner, Stefan Wildermann, Deepak Gangadharan, Michael Glaß, and Jürgen Teich. “A design-time/run-time application mapping methodology for predictable execution time in MPSoCs”. In: *ACM Transactions on Embedded Computing Systems (TECS)* 17.5 (2018), p. 89.
- [80] Jürgen Teich, Jörg Henkel, Andreas Herkersdorf, Doris Schmitt-Landsiedel, Wolfgang Schröder-Preikschat, and Gregor Snelting. “Invasive computing: An overview”. In: *Multiprocessor System-on-Chip*. Springer, 2011, pp. 241–268.
- [81] Amit Kumar Singh, Akash Kumar, and Thambipillai Srikanthan. “A hybrid strategy for mapping multiple throughput-constrained applications on MPSoCs”. In: *2011 Proceedings of the 14th International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*. IEEE, 2011, pp. 175–184.
- [82] Wei Quan and Andy D Pimentel. “A hybrid task mapping algorithm for heterogeneous MPSoCs”. In: *ACM Transactions on Embedded Computing Systems (TECS)* 14.1 (2015), p. 14.
- [83] Andrés Goens, Robert Khasanov, Marcus Hähnel, Till Smejkal, Hermann Härtig, and Jeronimo Castrillon. “TETRIS: a Multi-Application Run-Time System for Predictable Execution of Static Mappings”. In: *Proceedings of the 20th International Workshop on Software and Compilers for Embedded Systems (SCOPES’17)*. SCOPES ’17. Sankt Goar, Germany: ACM, June 2017, pp. 11–20. ISBN: 978-1-4503-5039-6. DOI: [10.1145/3078659.3078663](https://doi.org/10.1145/3078659.3078663). URL: <http://doi.acm.org/10.1145/3078659.3078663>.
- [84] Andrés Goens, Sergio Siccha, and Jeronimo Castrillon. “Symmetry in Software Synthesis”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 14.2 (July 2017), 20:1–20:26. ISSN: 1544-3566. DOI: [10.1145/3095747](https://doi.org/10.1145/3095747). URL: <http://doi.acm.org/10.1145/3095747>.
- [85] Robert Khasanov and Jeronimo Castrillon. “Energy-efficient Runtime Resource Management for Adaptable Multi-application Mapping”. In: *Proceedings of the 2020 Design, Automation and Test in Europe Conference (DATE)*. DATE ’20. Grenoble, France: EDA Consortium, Mar. 2020.
- [86] Robert Khasanov, Julian Robledo, Christian Menard, Andres Goens, and Jeronimo Castrillon. “Domain-specific hybrid mapping for energy-efficient baseband processing in wireless networks”. In: *ACM Transactions on Embedded Computing Systems (TECS), special issue of the 2021 International Conference on Compilers, Architecture, and Synthesis of Embedded Systems (CASES)* 20.5s (Sept. 2021). ISSN: 1539-9087. DOI: [10.1145/3476991](https://doi.org/10.1145/3476991). URL: <https://doi.org/10.1145/3476991>.
- [87] Hervé Yviquel, Alexandre Sanchez, Raullet Mickaël, and Emmanuel Casseau. *Multicore Runtime for Dynamic Dataflow Video Decoders*. Technical Report. IETR/INSA Rennes, IRISA, Inria Rennes, Apr. 2017. URL: <https://hal.archives-ouvertes.fr/hal-01503378>.
- [88] *Synopsys Signal Processing WorkSystem (SPW): The Fastest Path from Innovation to Implementation of Digital Signal Processing Systems*. URL: <http://www.eigen.in/pdf/SPW.pdf>.
- [89] *Synopsys System Studio*. URL: <https://news.synopsys.com/index.php?s=20295&item=123136>.
- [90] Enagnon Cedric Klikpo, Jad Khatib, and Alix Munier-Kordon. “Modeling multi-periodic simulink systems by synchronous dataflow graphs”. In: *2016 IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*. IEEE, 2016, pp. 1–10.
- [91] Thierry Goubier, Renaud Sirdey, Stéphane Louise, and Vincent David. “ ΣC : A programming model and language for embedded manycores”. In: *International Conference on Algorithms and Architectures for Parallel Processing*. Springer, 2011, pp. 385–394.
- [92] Benoit Dupont de Dinechin. “Dataflow language compilation for a single chip massively parallel processor”. In: *2013 IEEE 6th International Workshop on Multi-/Many-core Computing Systems (MuCoCoS)*. IEEE, 2013, pp. 1–1.
- [93] Konstantina Koliogeorgi, Nils Voss, Sotiria Fytraki, Sotirios Xydis, Georgi Gaydadjiev, and Dimitrios Soudris. “Dataflow acceleration of smith-waterman with traceback for high throughput next generation sequencing”. In: *2019 29th International Conference on Field Programmable Logic and Applications (FPL)*. IEEE, 2019, pp. 74–80.

- [94] Jianjiang Ceng, Weihua Sheng, Jeronimo Castrillon, Anastasia Stulova, Rainer Leupers, Gerd Ascheid, and Heinrich Meyr. “A High-level Virtual Platform for Early MPSoC Software Development”. In: *Proceedings of the 7th IEEE/ACM international conference on Hardware/software codesign and system synthesis (CODES+ISSS '09)*. Grenoble, France: ACM, Oct. 2009, pp. 11–20. ISBN: 978-1-60558-628-1. DOI: <http://doi.acm.org/10.1145/1629435.1629438>.
- [95] Rainer Leupers and Jeronimo Castrillon. “MPSoC Programming Using the MAPS Compiler”. In: *Proceedings of the Design Automation Conference (ASP-DAC), 2010 15th Asia and South Pacific*. Jan. 2010, pp. 897–902. DOI: [10.1109/ASPDAC.2010.5419677](https://doi.org/10.1109/ASPDAC.2010.5419677).
- [96] Jeronimo Castrillon, Stefan Schürmans, Anastasia Stulova, Weihua Sheng, Torsten Kempf, et al. “Component-based Waveform Development: The Nucleus Tool Flow for Efficient and Portable Software Defined Radio”. In: *Analog Integrated Circuits and Signal Processing* 69.2-3 (Dec. 2011), pp. 173–190. ISSN: 0925-1030. DOI: [10.1007/s10470-011-9670-1](https://doi.org/10.1007/s10470-011-9670-1). URL: <http://dx.doi.org/10.1007/s10470-011-9670-1>.
- [97] Jeronimo Castrillon and Rainer Leupers. *Programming Heterogeneous MPSoCs: Tool Flows to Close the Software Productivity Gap*. Springer, 2014, p. 258. ISBN: 978-3-319-00675-8. DOI: [10.1007/978-3-319-00675-8](https://doi.org/10.1007/978-3-319-00675-8).
- [98] Andrés Goens, Robert Khasanov, Jeronimo Castrillon, Simon Polstra, and Andy Pimentel. “Why Comparing System-level MPSoC Mapping Approaches is Difficult: a Case Study”. In: *Proceedings of the IEEE 10th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc-16)*. Ecole Centrale de Lyon, Lyon, France, Sept. 2016, pp. 281–288. DOI: [10.1109/MCSoc.2016.48](https://doi.org/10.1109/MCSoc.2016.48).
- [99] Heikki Orsila, Tero Kangas, Erno Salminen, Timo D. Hämäläinen, and Marko Hännikäinen. “Automated memory-aware application distribution for multi-processor system-on-chips”. In: *J. of Sys. Arch.* 53.11 (2007), pp. 795–815.
- [100] Sorin Manolache, Petru Eles, and Zebo Peng. “Task mapping and priority assignment for soft real-time applications under deadline miss ratio constraints”. In: *ACM Transactions on Embedded Computing Systems (TECS)* 7.2 (2008), pp. 1–35.
- [101] Cagkan Erbas, Selin Cerav-Erbas, and Andy D Pimentel. “Multiobjective optimization and evolutionary algorithms for the application mapping problem in multiprocessor system-on-chip design”. In: *IEEE Transactions on Evolutionary Computation* 10.3 (2006), pp. 358–374.
- [102] Robert Dick. *Embedded Systems Synthesis Benchmark Suite (e3s)*. 2008. URL: <http://ziyang.eecs.umich.edu/%5C%7B%7Ddickrp/e3s/>.
- [103] Tobias Schwarzer, Andreas Weichslgartner, Michael Glaß, Stefan Wildermann, Peter Brand, and Jürgen Teich. “Symmetry-eliminating design space exploration for hybrid application mapping on many-core architectures”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 37.2 (2017), pp. 297–310.
- [104] Kalray inc. *Kalray MPPA3 Coolidge Announcement*. 2020. URL: <https://www.kalrayinc.com/release-of-third-generation-mppa-processor-coolidge/>.
- [105] Marten Lohstroh, Íñigo Incer Romero, Andrés Goens, Patricia Derler, Jeronimo Castrillon, Edward A. Lee, and Alberto Sangiovanni-Vincentelli. “Reactors: A Deterministic Model for Composable Reactive Systems”. In: *Cyber Physical Systems. Model-Based Design – Proceedings of the 9th Workshop on Design, Modeling and Evaluation of Cyber Physical Systems (CyPhy 2019) and the Workshop on Embedded and Cyber-Physical Systems Education (WESE 2019)*. Ed. by Roger Chamberlain, Martin Edin Grimheden, and Walid Taha. New York City, NY, USA: Springer International Publishing, Feb. 2020, pp. 59–85. ISBN: 978-3-030-41131-2. DOI: [10.1007/978-3-030-41131-2_4](https://doi.org/10.1007/978-3-030-41131-2_4). URL: https://link.springer.com/chapter/10.1007/978-3-030-41131-2_4.
- [106] Christian Menard, Andrés Goens, Marten Lohstroh, and Jeronimo Castrillon. “Achieving Determinism in Adaptive AUTOSAR”. In: *Proceedings of the 2020 Design, Automation and Test in Europe Conference (DATE)*. DATE '20. Grenoble, France: EDA Consortium, Mar. 2020.
- [107] Julien Heulot, Maxime Pelcat, Karol Desnos, Jean-Francois Nezan, and Slaheddine Aridhi. “Spider: A synchronous parameterized and interfaced dataflow-based rtos for multicore dsp”. In: *2014 6th European Embedded Design in Education and Research Conference (EDERC)*. IEEE. 2014, pp. 167–171.
- [108] Hamza Deroui, Karol Desnos, Jean-François Nezan, and Alix Munier-Kordon. “Relaxed subgraph execution model for the throughput evaluation of IBSDF graphs”. In: *2017 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)*. IEEE. 2017, pp. 213–220.
- [109] Simon Holmbacka, Erwan Nogues, Maxime Pelcat, Sébastien Lafond, and Johan Lilius. “Energy efficiency and performance management of parallel dataflow applications”. In: *Proceedings of the 2014 Conference on Design and Architectures for Signal and Image Processing*. IEEE. 2014, pp. 1–8.

- [110] Karol Desnos, Maxime Pelcat, Jean-François Nezan, and Slaheddine Aridhi. “Distributed memory allocation technique for synchronous dataflow graphs”. In: *2016 IEEE International Workshop on Signal Processing Systems (SiPS)*. IEEE. 2016, pp. 45–50.
- [111] Julien Hascoët, Karol Desnos, Jean-François Nezan, and Benoit Dupont de Dinechin. “Hierarchical dataflow model for efficient programming of clustered manycore processors”. In: *2017 IEEE 28th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*. IEEE. 2017, pp. 137–142.
- [112] Bart Kienhuis, Ed F Deprettere, Pieter Van der Wolf, and Kees Visser. “A methodology to design programmable embedded systems”. In: *International Workshop on Embedded Computer Systems*. Springer. 2001, pp. 18–37.
- [113] J. Sérot. “HoCL: High level specification of dataflow graphs”. In: *Proceedings of the 32nd International Symposium on Implementation and Application of Functional Languages (IFL 2020)*. U. of Kent, Sept. 2020, pp. 244–253. URL: <https://www.cs.kent.ac.uk/events/2020/ifl20/ifl2020draftproceedings.pdf>.
- [114] Maxime Pelcat, Jean François Nezan, Jonathan Piat, Jerome Croizer, and Slaheddine Aridhi. “A System-Level Architecture Model for Rapid Prototyping of Heterogeneous Multicore Embedded Systems”. In: *Conference on Design and Architectures for Signal and Image Processing (DASIP) 2009*. nice, France, Sept. 2009, 8 pages. URL: <https://hal.archives-ouvertes.fr/hal-00429397>.
- [115] Julien Heulot, Jani Boutellier, Maxime Pelcat, Jean-François Nezan, and Slaheddine Aridhi. “Applying the adaptive Hybrid Flow-Shop scheduling method to schedule a 3GPP LTE physical layer algorithm onto many-core digital signal processors”. In: *2013 NASA/ESA Conference on Adaptive Hardware and Systems (AHS-2013)*. IEEE. 2013, pp. 123–129.
- [116] J. Heulot, M. Pelcat, J. Nezan, Y. Oliva, S. Aridhi, and S. S. Bhattacharyya. “Just-in-time scheduling techniques for multicore signal processing systems”. In: *2014 IEEE Global Conference on Signal and Information Processing (GlobalSIP)*. 2014, pp. 25–29. DOI: [10.1109/GlobalSIP.2014.7032071](https://doi.org/10.1109/GlobalSIP.2014.7032071).
- [117] Florian Arrestier, Karol Desnos, Eduardo Juarez, and Daniel Menard. “Numerical Representation of Directed Acyclic Graphs for Efficient Dataflow Embedded Resource Allocation”. In: *ACM Trans. Embed. Comput. Syst.* 18.5s (Oct. 2019). ISSN: 1539-9087. DOI: [10.1145/3358225](https://doi.org/10.1145/3358225). URL: <https://doi.org/10.1145/3358225>.
- [118] Claudius Ptolemaeus, ed. *System Design, Modeling, and Simulation using Ptolemy II*. Ptolemy.org, 2014. URL: <http://ptolemy.org/books/Systems>.
- [119] Jeronimo Castrillon, Matthias Lieber, Sascha Klüppelholz, Marcus Völp, Nils Asmussen, et al. “A Hardware/Software Stack for Heterogeneous Systems”. In: *IEEE Transactions on Multi-Scale Computing Systems* 4.3 (July 2018), pp. 243–259. ISSN: 2332-7766. DOI: [10.1109/TMSCS.2017.2771750](https://doi.org/10.1109/TMSCS.2017.2771750). URL: <http://ieeexplore.ieee.org/document/8103042/>.
- [120] Gerhard Fettweis, Meik Dörpinghaus, Jeronimo Castrillon, Akash Kumar, Christel Baier, et al. “Architecture and Advanced Electronics Pathways Towards Highly Adaptive Energy-Efficient Computing”. In: *Proceedings of the IEEE* 107.1 (Jan. 2019), pp. 204–231. ISSN: 0018-9219. DOI: [10.1109/JPROC.2018.2874895](https://doi.org/10.1109/JPROC.2018.2874895). URL: <https://ieeexplore.ieee.org/document/8565890>.