cfaed Colloquium

DATE: 27 September 2019
TIME: 9:25 am
LOCATION: TU Dresden, Barkhausen-Bau (BAR), Heinz-Schönfeld-Hörsaal BAR I90, Georg-Schumann-Str. 13, 01187 Dresden

SPEAKER: **Prof. Dr.-Ing. Thomas Mikolajick**
NaMLab gGmbH
Chair of Nanoelectronic Materials, TU Dresden

TITLE: ***"Reconfigurable Nanowire Electronics – A Path beyond Moore´s Law"***

Abstract:
Reconfigurable devices are a possibility to achieve more functionality of integrated circuits at a given device count. Therefore such devices are one option to increase the system complexity without or drastically reduced further device scaling. The silicon nanowire path was based on the RFET concept first reported shortly before the beginning of the cluster of excellence cfaed [1]. During the seven years of cfaed, the technology was further developed towards making it usable for circuits. On the technology and device side, a symmetrical RFET device was demonstrated, to increase the complexity of lab demonstrators a top-down technology was developed, the inherent performance drawback of Schottky barrier devices was attacked by using Germanium as the channel material and in the last phase of the cluster first demonstrations of nonvolatile RFETs have been achieved. On the circuit and system side the step from device to simple circuits has been taken, compact models have been developed and later more complex circuits, showing the benefit of the concept were demonstrated together with the first version of a CAD environment. Finally the device concept was extend to transducers for chemical and biochemical sensors by using parallel nanowire devices with many parallel nanowires to increase the sensing current. Thee type of devices can be reconfigured in the final fabrication step by adding sensitive layers to realize different sensors. As highlights a flexible sensor or birds Flu as well as a sensor array co-integrated with CMOS circuits were realized. Looking forward, the addition of Nonvolatility will open up additional reconfiguration options. Finally the implementation of such a complex approach, that needs innovations on all abstraction layer calls for a stepwise approach. Hardware security could be a first application were the RFET device is co-integrated with classical CMOS.